

## PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2002-289653

(43)Date of publication of application : 04.10.2002

(51)Int.Cl.

H01L 21/60  
C23C 18/31  
C23C 18/54  
C23C 28/00  
C23C 30/00

(21)Application number : 2001-086913

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(22)Date of filing : 26.03.2001

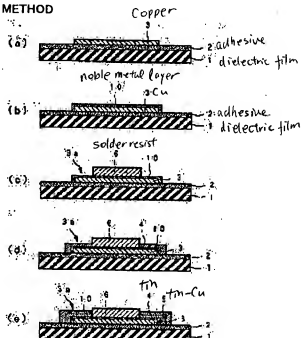
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## (54) SEMICONDUCTOR DEVICE TAPE CARRIER AND ITS MANUFACTURING METHOD

(57)Abstract:

**PROBLEM TO BE SOLVED:** To prevent excess melting of copper of a lead wire in a lower part of a solder resist and suppress the whisker of tin plating in a semiconductor device tape carrier.

**SOLUTION:** A noble metal plated layer of such as silver, gold and palladium 10 is formed on a copper foil wiring pattern 3 which is formed on an dielectric film 1 via an adhesive layer 2, thereafter, the solder resist 8 is applied in a position except a terminal portion of the wiring pattern 3, and a tin-plated layer is formed on the terminal portion. Then, a tin-copper alloy 5 of 0.20  $\mu\text{m}$  or more in thickness and a pure tin layer 4 of 0.15 to 0.80  $\mu\text{m}$  in thickness are formed by heat treatment.



## LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

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CLAIMS

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## [Claim(s)]

[Claim 1] The tape carrier for semiconductor devices characterized by forming a tin-copper alloy layer with a thickness of 0.20 micrometers or more and a pure tin layer with a thickness of 0.15-0.80 micrometers by performing noble-metals plating, such as silver, gold, and palladium, applying a solder resist to the position except a part for the terminal area of said circuit pattern, and forming and heat-treating a tinning layer to a part for said terminal area on the circuit pattern of the copper foil given through the adhesives layer on the insulating film.

[Claim 2] The tape carrier for semiconductor devices according to claim 1 characterized by setting thickness of said noble-metals plating to 0.1 micrometers or less in the tape carrier for semiconductor devices according to claim 1.

[Claim 3] On the circuit pattern of the copper foil given through the adhesives layer on the insulating film By applying a solder resist to the position except a part for the terminal area of said circuit pattern, after performing noble-metals plating, such as silver, gold, and palladium, forming a tinning layer in a part for said terminal area after that, and heat-treating after that The manufacture approach of the tape carrier for semiconductor devices characterized by forming a tin-copper alloy layer with a thickness of 0.20 micrometers or more and a pure tin layer with a thickness of 0.15-0.80 micrometers.

[Claim 4] The manufacture approach of the tape carrier for semiconductor devices characterized by setting thickness of said noble-metals plating to 0.1 micrometers or less in the manufacture approach according to claim 3.

[Claim 5] The manufacture approach of the tape carrier for semiconductor devices characterized by performing said tinning with nonelectrolytic plating in the manufacture approach according to claim 3 or 4.

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DETAILED DESCRIPTION

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[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the tape career and the tinning technique of a tape career for semiconductor devices like the TAB tape career which is precision electronic parts, and the structure which faced performing tinning to the circuit pattern of the copper foil especially, and prevented \*\*\*\*\* of the copper in the solder resist case.

[0002]

[Description of the Prior Art] The structure of the conventional TAB tape career forms the predetermined circuit pattern 3 in the copper foil stuck on the insulation film 1 made of polyimide resin through the adhesives layer 2, as shown in drawing 2 ( drawing 2 (a)). On the circuit pattern 3, at the position except parts for a terminal area, such as the copper lead 3a Carry out printing spreading of the solder resist 6 as an insulating layer ( drawing 2 R> 2 (b)), and after that, in order to give the junction nature stabilized in copper lead 3a which is a part for the terminal area of the circuit pattern 3 concerned It is the structure ( drawing 2 (d)) which formed the pure tinning layer 4 by non-electrolyzed tinning ( drawing 2 (c)), and formed the tin-copper alloy layer 5 by heat-treatment.

[0003] As shown in drawing 3, a semiconductor device (IC chip) 7 is arranged so that it may be located in a device hole, and after the mounting activity to the semiconductor device of this TAB tape career carries out alignment of the electrode of a semiconductor device 7 to the inner lead projected in the device hole, it is stuck by pressure with a bonding tool. The golden bump 8 is formed in the electrode of a semiconductor device 7, if it is stuck to copper lead 3a by pressure in the condition of having been heated, tinning will fuse, a golden-tin alloy will form and an inner lead will be joined to an electrode.

[0004]

[Problem(s) to be Solved by the Invention] Generally, since tinning is excellent in corrosion resistance and soldering nature, it is widely used for electronic parts.

[0005] However, in the above-mentioned conventional TAB tape career, in case non-electrolyzed \*\*\*\*\* is carried out, as shown in drawing 4 R> 4, in the case of the lower part of a solder resist 6, copper carries out the superfluous dissolution in the section (edge), the part (superfluous dissolution section 9) corroded to copper lead 3a at the groove is formed, and there is a problem of reducing lead reinforcement.

[0006] Although non-electrolyzed tinning generally deposits in a permutation with copper, the pretreatment liquid of non-electrolyzed tinning cannot permeate easily in this case, the residue of the organic substance, a contamination, etc. remain in a copper front face, a reaction rate becomes early remarkably at the time of non-electrolyzed tinning, and copper dissolves a solder resist lower part superfluously.

[0007] A difference arises in a reaction rate at the time of non-electrolyzed tinning in the large place of plating area since the demand of the formation of a detailed circuit pattern is strong recently and plating area is furthermore smaller, and a detailed part. Especially, in the detailed section, the reaction rate of non-electrolyzed tinning becomes early, copper carries out the superfluous dissolution, and lead

reinforcement falls.

[0008] As other troubles, since it is known well that whiskers (mustache-like crystal) will generate it if a tinning coat is left immediately after tinning and generating of whiskers becomes a short cause by the pattern of a detailed pitch especially, various examination has been performed. As a control means of these tin whiskers, it is (1). As substrate plating, a nickel, copper, lead, solder, tin-nickel alloy, and tin-copper alloy layer is formed. (2) Perform reflow processing after plating. (3) Heat after plating and perform annealing treatment. \*\* is known.

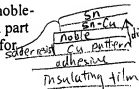
[0009] However, the above (1) Since a substrate plating process is given, as for the technique of performing substrate plating, cost becomes high. Above (2) Even if the method of performing reflow processing after plating performs thick uniform plating first, variation arises in plating thickness and the problem that a tinning front face oxidizes further produces after a reflow. Although the approach of performing annealing treatment after the plating of the above (3) has whiskers depressor effect for a short period of time, since growth of whiskers cannot be completely prevented if the long period of time of about six months comes, there is a problem that it does not become a perfect cure against whiskers.

[0010] Then, the purpose of this invention is to offer the tape carrier for semiconductor devices and its manufacture approach of the tinning structure that the whiskers of tinning can be controlled cheaply, without spoiling the property of tinning and of having high dependability while it solves the above-mentioned technical problem and prevents \*\*\*\*\* of the superfluous dissolution of the copper of lead wiring of a solder resist lower part, i.e., the copper in the solder resist case.

[0011]

[Means for Solving the Problem] In order to attain the above-mentioned purpose, this invention is constituted as follows.

[0012] (1) The tape carrier for semiconductor devices concerning invention of claim 1 On the circuit pattern of the copper foil given through the adhesives layer on the insulating film By performing noble-metals plating, such as silver, gold, and palladium, applying a solder resist to the position except a part for the terminal area of said circuit pattern, and forming and heat-treating a tinning layer to a part for said terminal area It is characterized by forming a tin-copper alloy layer with a thickness of 0.20 micrometers or more and a pure tin layer with a thickness of 0.15-0.80 micrometers.



[0013] (2) Invention of claim 2 is characterized by setting thickness of said noble-metals plating to 0.1 micrometers or less in the tape carrier for semiconductor devices according to claim 1.

[0014] (3) The manufacture approach of the tape carrier for semiconductor devices concerning invention of claim 3 On the circuit pattern of the copper foil given through the adhesives layer on the insulating film By applying a solder resist to the position except a part for the terminal area of said circuit pattern, after performing noble-metals plating, such as silver, gold, and palladium, forming a tinning layer in a part for said terminal area after that, and heat-treating after that It is characterized by forming a tin-copper alloy layer with a thickness of 0.20 micrometers or more and a pure tin layer with a thickness of 0.15-0.80 micrometers.

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[0015] (4) Invention of claim 4 is characterized by setting thickness of said noble-metals plating to 0.1 micrometers or less in the manufacture approach according to claim 3.

[0016] (5) In the manufacture approach according to claim 3 or 4, it is characterized by performing said tinning with nonelectrolytic plating.

[0017]

[Embodiment of the Invention] Hereafter, this invention is explained based on the operation gestalt of illustration.

[0018] The manufacture approach of the TAB tape carrier as an example of the tape carrier for semiconductor devices by this invention is shown in drawing 1. First, by performing etching, after making the photo mask which has a predetermined wiring lead pattern after applying a predetermined photoresist to the tape carrier which formed copper foil through the adhesives layer 2 on the insulation film 1 made of polyimide resin and drying it let pass and expose and develop, as shown in drawing 1 (a), the predetermined detailed circuit pattern 3 is produced.

[0019] Next, as shown in drawing 1 (b), the noble-metals plating layers 10, such as silver with a

thickness of 0.01-0.1 micrometers, gold, and palladium, are formed on the circuit pattern 3 of this copper foil.

[0020] Subsequently, as shown in drawing 1 (c), a solder resist 6 is applied to the part on the circuit pattern 3 with which this noble-metals plating layer 10 was formed, i.e., the position except parts for a terminal area, such as copper lead 3a, by print processes.

[0021] As shown in drawing 1 (d), next, to a part for the above-mentioned terminal area of this tape career (copper lead 3a etc.) That is, by forming the tinning layer 4 on the noble-metals plating layer 10, and carrying out 100-150 degrees C and heat-treatment for 5 minutes - 90 minutes after that Copper is diffused in the tinning layer concerned, and as shown in drawing 1 R> 1 (e), the copper diffusion tinning layer, the tinning layer 4, i.e., the pure tin layer, with a thickness of 0.15-0.80 micrometers which does not contain copper substantially, 5 with a thickness of 0.20 micrometers or more, i.e., a tin-copper alloy layer, is formed.

next-treatment

[0022] Thus, the noble-metals plating layers 10, such as silver, gold, and palladium, are formed previously, parts for a terminal area, such as copper lead 3a, are covered with this noble-metals plating layer 10, and, as for the TAB tape career formed, a solder resist 6 is formed on it. For this reason, since the copper front face is covered with the noble-metals plating layer 10 and copper foil does not contact plating liquid even if plating liquid trespasses upon the inferior surface of tongue of a solder resist 6 in the case of tinning processing, local electric corrosion does not happen. Therefore, the superfluous dissolution section 9 of the copper shown in drawing 4 is not formed in copper lead 3a. Therefore, it can lose un-arranging [ that the copper superfluous dissolution section 9 exists in copper lead 3a, and the reinforcement of copper lead 3a becomes weaker ].

[0023] As for the thickness of the noble-metals plating layer 10, in the above-mentioned manufacture approach of a TAB tape career, it is desirable that it is 0.1 micrometers or less. It is because the whole surface is covered and carries out stripes with noble-metals plating mostly, time amount will be taken before non-electrolyzed tinning liquid attains even the copper of a substrate through a pinhole and a deposit rate will fall, in case it deposits through the pinhole of a noble-metals plating coat at the time of non-electrolyzed tinning if the thickness of this noble-metals plating layer 10 exceeds 0.1 micrometers.

[0024] If the reason for having set thickness of the pure tin layer 4 to 0.15-0.80 micrometers becomes difficult [ the bonding nature of an inner lead ] in the case of less than 0.15 micrometers on the other hand and 0.8 micrometers is exceeded -- plating -- it is because who is produced and it becomes the cause of a short circuit. Moreover, the reason for having set thickness of the tin-copper alloy layer 5 by the 2nd tinning processing to 0.20 micrometers or more is that whiskers depressor effect becomes inadequate in the case of less than 0.20 micrometers.

[0025] As shown in drawing 3, a semiconductor device (IC chip) 7 is arranged so that it may be located in a device hole, and after the mounting activity to the semiconductor device of the above-mentioned TAB tape career carries out alignment of the electrode of a semiconductor device 7 to the inner lead projected in the device hole, it is stuck by pressure with a bonding tool. The golden bump 8 is formed in the electrode of a semiconductor device 7, if it is stuck to copper lead 3a by pressure in the condition of having been heated, tinning will fuse, a golden-tin alloy will form and an inner lead will be firmly joined to an electrode.

[0026]

[Example] After making the photo mask which has a predetermined wiring lead pattern after applying a predetermined resist to the tape career of 25 micrometers of copper foil formed through the adhesives layer 2 on the insulation film 1 made of polyimide resin and drying it let pass and expose and develop, the lead pattern was produced by performing etching.

[0027] And first, on the copper circuit pattern of the tape career for semiconductor devices with which the copper detailed pattern was formed on the insulation film 1 made of polyimide resin, after performing silver plating with a thickness of 0.01-0.25 micrometers and printing a solder resist 6 to the part on the circuit pattern, about 0.5-micrometer tinning layer was formed and the pure tin layer 4 and the tin-copper alloy layer 5 were formed by heat-treatment at 100 degrees C - 150 degrees C for 5 minutes - 90 minutes. Here, the thing in which 0.2-0.3 micrometers and 0.15-0.20 micrometers of tin-

copper alloy layers 5 were made to form the pure tin layer 4 by heat-treatment was produced.  
 [0028] Although tinning could be formed by the approach of either electrolysis and nonelectrolytic plating, it was taken as nonelectrolytic plating at the point with little variation in plating thickness here.  
 [0029] Non-electrolyzed tinning liquid was processed in 70 degrees C and 5-500s using ISHIHARA CHEMICAL 580M. Thus, about the produced sample, copper superfluous soluble evaluation was performed by cross-section observation. This result is shown in Table 1 as tinning conditions and an overcopper solubility evaluation result.

[0030]

[Table 1]

スズめっき条件と銅過剰溶解性評価結果

サンプル	1 回目 Ag めっき厚	2 回目めっき厚		銅過剰溶解性評価結果
		合金層厚	純スズ厚	
1	0	0.22	0.35~0.4	×
2	0.01	0.22	0.25~0.3	○
3	0.05	0.22	0.25~0.3	○
4	0.10	0.22	0.25~0.3	○
5	0.15	0.18	0.15~0.2	○
6	0.20	0.15	0.10~0.15	○

[0031] As shown in Table 1, as for the superfluous dissolution of copper, neither of the samples which carried out Ag plating to the substrate was observed. That is, it is thought that the superfluous dissolution of copper can prevent it if the thickness of a silver plating layer (noble-metals plating layer 10) is at least 0.01 micrometers or more. Moreover, since the deposit rate of tinning will fall if silver plating thickness exceeds 0.1 micrometers, silver plating thickness has desirable 0.1 micrometers or less.

[0032] The superfluous dissolution of copper was observed at the case which carried out non-electrolyzed tinning after solder resist printing like a sample 1 on the other hand.

[0033] Next, about 150 inner leads after measuring pure tinning thickness with a KOKURU meter, measuring all tin thickness by the fluorescence-X-rays thickness gage, deducting and carrying out (pure tin thickness) from (all tin thickness) and asking for and carrying out neglect of the thickness of a tin-copper alloy layer in one to June (30 days, 60 days, 90 days, 180 days), whiskers were observed with the 200 times as many optical microscope as this, respectively, and the occurrences of the whiskers were counted. This tinning condition, tinning thickness, and a whiskers nature evaluation result are shown in Table 2. It was observed that whiskers occurrences increase as shown in Table 2 and lapsed days increased, when a tin-copper alloy layer was less than (samples 2, 5, 8, 11, and 14) 0.20 micrometers. Thereby, it turns out that there is effectiveness which controls the whiskers of tin, so that the diffusion layer of tin-copper is thick.

[0034]

[Table 2]

スズめっき条件とスズめっき厚、ホイスカ試験結果

サンプル	1 回目めっき厚	2 回目めっき厚		ホイスカ試験結果			
		合金層厚	純スズ厚	30 日	60 日	90 日	180 日
1	0	0.22	0.35~0.4	0	0	0	0
2	0.01	0.15	0.25~0.3	2	5	10	15
3	↑	0.20	0.25~0.3	0	0	0	0
4	↑	0.25	0.25~0.3	0	0	0	0
5	0.05	0.15	0.25~0.3	1	6	11	17
6	↑	0.20	0.25~0.3	0	0	0	0
7	↑	0.25	0.25~0.3	0	0	0	0
8	0.10	0.15	0.25~0.3	3	7	10	25
9	↑	0.20	0.25~0.3	0	0	0	0
10	↑	0.25	0.25~0.3	0	0	0	0
11	0.15	0.15	0.15~0.2	2	7	20	31
12	↑	0.20	0.15~0.2	0	0	0	0
13	↑	0.25	0.15~0.2	0	0	0	0
14	0.20	0.15	0.10~0.15	4	12	28	36
15	↑	0.20	0.10~0.15	0	0	0	0
16	↑	0.25	0.10~0.15	0	0	0	0

[0035] Although the tape carrier of 25 micrometers of copper foil was used in the above-mentioned example, when it replaced with this and the same evaluation as the above was performed by the tape carrier of 10 micrometers of copper foil, the 1st \*\*\*\*\* thickness did not generate copper superfluous lysis in 0.10 micrometers or less.

[0036] Moreover, after performing gold or palladium plating to substrate plating similarly like the above-mentioned example, when it evaluated, the same result as Table 1 of the above-mentioned example and Table 2 was obtained.

[0037]

[Effect of the Invention] As explained above, according to this invention, the following outstanding effectiveness is acquired.

[0038] According to the tape carrier for semiconductor devices and its manufacture approach of this invention, on the circuit pattern of the copper foil given through the adhesives layer on the insulating film By applying a solder resist to the position except a part for the terminal area of said circuit pattern, after performing noble-metals plating, such as silver, gold, and palladium, forming a tinning layer in a part for said terminal area after that, and heat-treating after that A tin-copper alloy layer with a thickness of 0.20 micrometers or more and a pure tin layer with a thickness of 0.15-0.80 micrometers are formed.

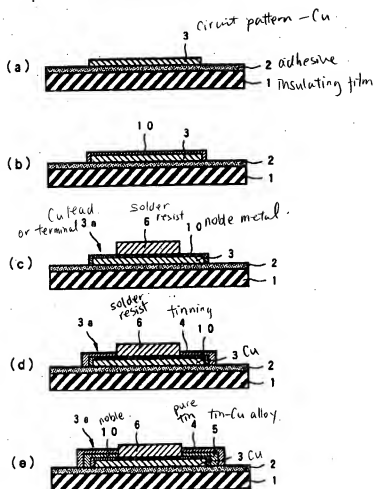
[0039] Noble-metals plating layers, such as silver, gold, and palladium, are formed previously, parts for a terminal area, such as a copper lead, are covered with this noble-metals plating layer, and a solder resist is formed in the part on that noble-metals plating layer. For this reason, since the copper front face is covered with the noble-metals plating layer and copper foil does not contact plating liquid even if plating liquid trespasses upon the inferior surface of tongue of a solder resist in the case of tinning processing, local electric corrosion does not happen. Therefore, the copper superfluous dissolution section is not formed in a copper lead. Therefore, it can lose un-arranging [ that the copper superfluous dissolution section exists in a copper lead, and the reinforcement of a copper lead becomes weaker ].

[0040] furthermore -- since the pure tin layer is set to 0.15-0.80 micrometers in the 2nd tinning processing -- the bonding nature of an inner lead -- good -- and plating -- who is not produced. Moreover, since the 2nd tin-copper alloy layer is set to 0.20 micrometers or more, sufficient whiskers

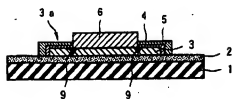
depressor effect can be acquired.

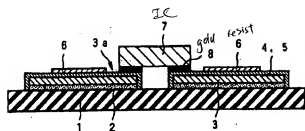
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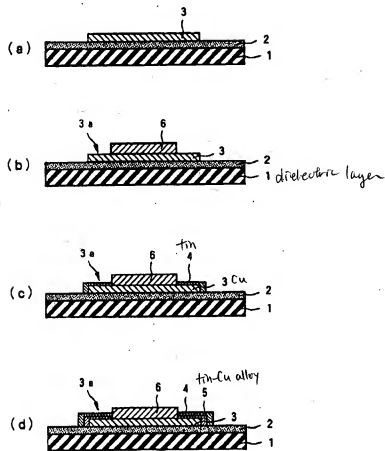
[Translation done.]



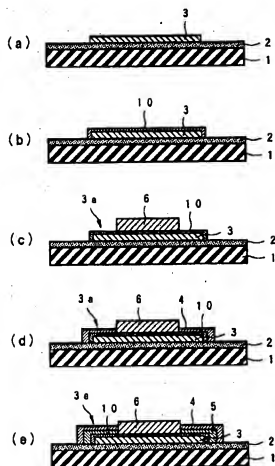
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